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METHOD AND APPARATUS FOR READ BITLINE CLAMPING FOR GAIN CELL DRAM DEVICES

Abstract

A dynamic random access memory (DRAM) storage device includes a storage cell having a plurality of transistors arranged in a gain cell configuration, the gain cell coupled to a read bitline and a write bitline. A dummy cell is configured as a clamping device for the read bitline, wherein the dummy cell opposes a read bitline voltage swing during a read operation of the storage cell.